APPENDIX A: AMENDMENT WORKSHEET

IN THE SPECIFICATION:

The first full paragraph on page 14:

"In still a further preferred embodiment of the present invention, Figures 6-13 show**[s]** the use of a blind via 148 to house electrically connected **[intermediate]** **passive** components 114 within an integrated passive device 150. In such an embodiment, the vias 148 contain various passive components 114 as discussed above which serve in addition to their electrical functions as connections between other of the passive components comprising the device 150. In this manner, the footprint of an IPD may be reduced while providing greater flexibility in its design layout."

The first full paragraph on page 15:

"With the basic construction of the device's skeletal frame 150 completed, as can be seen in Figure 9, the manufacturer is now able to form the additional resistive/conductive patterns 158 required on an outer surface of the device and band terminate the edges to provide **[points of electrical connection]** **terminations** 160 for such device. The methods of making such patterns 158 and terminations 160 are varied but generally known in the art. They form no particular aspect of the present invention and therefore will not be explained in detail."

The first full paragraph on page 16:

"In order to ensure both the electrical and physical stability of the passive component 114, the vias 148 may be filled with an insulating epoxy 166 or other similar material to partially encase the passive component 114 and hold it in place. As **[discussed above and as]** seen in Figure **[12]** **13**, if the conductor patterns have been formed either by thin-film plating or thick-film printing, the electrical connection to the upper conductor 164 may then be formed by filling in the remaining portion of the via 148 either with a conductor or a solder paste **118** and either cure or reflow it, respectively."

IN THE CLAIMS:

19. (Amended) A multi-layer **[electronic]** **electrical** device comprising:

a first device layer with a first series of resistive/conductive patterns thereon;

a second device layer with a plurality of via drilled therethrough;

a unitary device body formed by the bonded union of the first and second device layers, wherein said via correspond to a respective capture pad in said first series of resistive/conductive patterns;

a second series of resistive/conductive patterns on an outer layer of said unitary body;

a plurality of terminations on said unitary body for electrical connection between other electronic devices and components of said device;

individual passive components **with first and second opposing electrical terminations, wherein each said individual passive component is** vertically mounted into **[each]** **a selected** of said plurality of via and **wherein one of said first and second opposing electrical terminations is** bonded to **[its]** **the** respective capture pad **for said selected of said plurality of via**;

multiple portions of a non-conductive material respectively substantially filling the space between each of said individual passive components and the surrounding via, wherein said non-conductive material partially encases each said individual passive component to hold it in place while leaving one of said first and second opposing electrical terminations exposed and prevents shorting between respective first and second opposing electrical terminations; and

an electrical connection between each of said passive components and at least a portion of said second series of resistive/conductive patterns on said outer surface of said unitary device body.

20. The multi-layer electrical device of claim 19, wherein said first and second layer are made of FR4.

21. The multi-layer electrical device of claim 20, wherein said device is a printed circuit board.

22. The multi-layer electrical device of claim 19, wherein said first and second layers are made of a non-conductive ceramic.

23. (Amended) The multi-layer electrical device of claim 22, wherein said device is an integrated passive component.

24. The multi-layer electrical device of claim 19, wherein said passive components comprise any combination of resistors, capacitors, varistors, and thermistors.

25. (Amended) A multi-layer electronic device comprising:

a plurality of first device layers, each such layer having a first series of resistive/conductive patterns thereon and a plurality of via drilled therethrough;

a plurality of second device layers, each such layer having a plurality of via drilled therethrough;

a unitary device body formed by the bonded union of an interleaved stack of said plurality of first and said second device layers, wherein each of said via correspond to a respective portion of the resistive/conductive patterns on the underlying device layer and wherein one of said second device layers forms the uppermost device layer and the lowermost device layer is one of said first device layers;

a second series of resistive/conductive patterns on an outer layer of said uppermost device layer;

a plurality of terminations on said unitary body for electrical connection between other electronic devices and various of the resistive/conductive patterns throughout said unitary device body;

individual passive components with respective first and second opposing terminations, wherein each individual passive component is vertically mounted into a selected of said plurality of via and wherein one of said first and second opposing

terminations are electrically connected to a portion of said underlying first device layer's first series of resistive/conductive patterns;

multiple portions of a non-conductive material respectively substantially filling the space between each of said individual passive components and the surrounding via, wherein said non-conductive material partially encases each said individual passive component to hold it in place while leaving one of said first and second opposing electrical terminations exposed and prevents shorting between respective first and second opposing electrical terminations; and

an electrical connection between each of said passive components and at least a portion of said overlying first device layer's first series of resistive/conductive patterns through a corresponding one of said first device layer's plurality of via.